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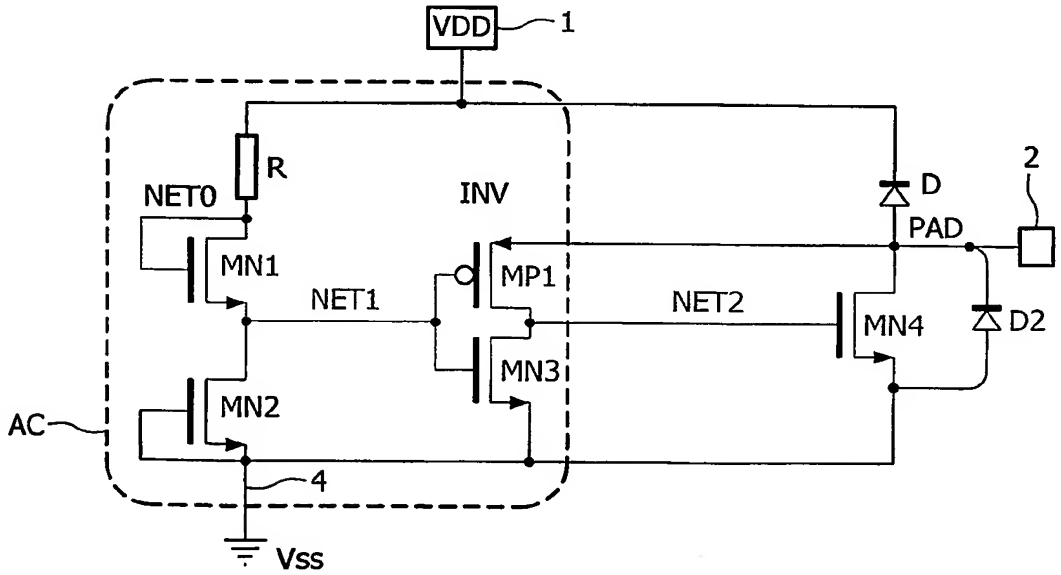
(54) Title: PROTECTION CIRCUIT FOR AN INTEGRATED CIRCUIT DEVICE



(57) Abstract: The integrated protection circuit according to the invention for ESD protecting an circuit device having at least one pad, e.g. a I/O pad, comprises a first transistor (MP1) whose control outputs are connected between the pad (2, 3) and the control input of a clamp transistor (MN4). The control outputs of the clamp transistor (MN4) are connected between the pad (2, 3) and a reference terminal (4). The protection circuit further comprises a second transistor (MN3) whose control outputs are connected between the control output of the first transistor (.MP 1) and the reference terminal (4). Finally the protection circuit also comprises time-delay elements (R, MN 1) connected between a supply voltage terminal (1) and the control inputs of the first transistor (MP I) and the second transistor (MN3).

WO 2005/002019 A1

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